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"ENCAPSULATED INTEGRATED CIRCUIT PACKAGE AND METHOD OF MANUFACTURING AN INTEGRATED CIRCUIT PACKAGE"

FIELD OF THE INVENTION

The present invention relates to integrated circuit packaging and manufacturing thereof, and more particularly, to integrated circuit packaging for improved dissipation of thermal energy.

BACKGROUND OF THE INVENTION

A semiconductor device generates a great deal of heat during normal operation. As the speed of semiconductors has increased, so too has the amount of heat generated by them. It is desirable to dissipate this heat from an integrated circuit package in an efficient manner.

A heat sink is one type of device used to help dissipate heat from some integrated circuit packages. Various shapes and sizes of heat sink devices have been incorporated onto, into or around integrated circuit packages for improving heat dissipation from the particular integrated circuit package. For example, U.S. Patent No. 5,596,231 to Combs, entitled "High Power Dissipation Plastic Encapsulated Package For Integrated Circuit Die," discloses a selectively coated heat sink attached directly on to the integrated circuit die and to a lead frame for external electrical connections.

SUMMARY OF THE INVENTION

In one aspect, the invention features a method of manufacturing an integrated circuit package including providing a substrate having a first surface, a second surface opposite the first surface, a cavity through the substrate between the first and second surfaces and a conductive via extending through the substrate and electrically connecting the first surface of the substrate with the second surface of the substrate,

applying a strip to the second surface of the substrate, mounting a semiconductor die on the strip, at least a portion of the semiconductor die being disposed inside the cavity, encapsulating in a molding material at least a portion of the first surface of the substrate, and removing the strip from the substrate.

In another aspect, the invention features a method of manufacturing an integrated circuit package including providing a substrate having a first surface, a second surface opposite the first surface, a plurality of cavities, each said cavity through the substrate between the first and second surfaces, and a plurality of conductive vias, each said via extending through the substrate and electrically connecting the first surface of the substrate with the second surface of the substrate, applying a strip to the second surface of said substrate, mounting a plurality of semiconductor dies on the strip, at least a portion of each semiconductor die being disposed inside each cavity, encapsulating in a molding material at least a portion of the first surface of said substrate, and removing the strip from the substrate to expose a surface of each semiconductor die.

In a further aspect, the invention features an integrated circuit package including a substrate having a first surface, a second surface opposite the first surface, a cavity through the substrate between the first and second surfaces and a conductive via extending through the substrate and electrically connecting the first surface of the substrate with the second surface of the substrate, a semiconductor die electrically coupled with the conductive via, at least a portion of the semiconductor die being disposed inside the cavity of the substrate, an encapsulant material encapsulating a portion of the semiconductor die such that at least a portion of a surface of the semiconductor die is exposed.